Q.P. Code: 19CS0503 **R19**

Reg. No: | | | | | | | | | | |

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY:: PUTTUR

(AUTONOMOUS)

B.Tech I Year II Semester Regular Examinations October-2020

DIGITAL LOGIC DESIGN

(Common to CSE & CSIT)

Time: 3 hours Max. Marks: 60

(Answer all Five Units **5 x 12 = 60** Marks)

UNIT-I

1	**a**	Convert the following i)$(1AD)_{16}=(\ )_{10}$ ii) $(453)_8=(\ )_{10}$ iii) $(10110011)_2=(\ )_{10}$ iv) $(5436)_{10}=(\ )_{16}$	**6M**
	b	Express the Boolean function F=A+B'C as a sum of min-terms.	**6M**

OR

2	**a**	Prove the following identities A' B' C' + A' B C' + A B' C' + A B C' = C'.	**6M**
	b	A B + A B C + A' B + A B' C = B + A C.	**6M**

UNIT-II

3		Simplify the Boolean expression using K-map and implement using NAND gates. F(A,B,C,D) = ∑m(0,2,3,8,10,11,12,14)	**12M**

OR

4		Simplify the Boolean expression using K-MAP. F(A,B,C,D) = πM (3,5,6,7,11,13,14,15) .d(9,10,12)	**12M**

UNIT-III

5	**a**	Explain about Binary Half Adder.	**6M**
	b	Design and draw a full adder circuit.	**6M**

OR

6		Implement BCD to 7-segment decoder for common anode using 4:16 decoder.	**12M**

UNIT-IV

7	**a**	Explain the Logic diagram of JK flip-flop.	**6M**
	b	Explain about Shift Registers.	**6M**

OR

8		Explain the design of a 4 bit binary counter with parallel load in detail.	**12M**

UNIT-V

9		What is memory decoding? Explain about the construction of 4 X 4 RAM?	**12M**

OR

10	**a**	Write difference between PROM, PLA & PAL.	**6M**
	b	Implement the following Boolean expressions using ROM. F1(A,B,C)=Σ(m(0,2,4,7) F2(A,B,C)=Σm(1,3,5,7)	**6M**

*** END ***